CLAIMS

What is claimed is:

1. A method for evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal inhibits transitions on an output of said gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal allows transitions on said output of said gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

2. The method of claim 1, wherein:

said input comprises a gate input;

said first-type of signal and said second-type of signal comprise gating signals; and

said first-type of signal and said second-type of signal control whether pulses on a clock input of said logical gating device are propagated to said output of said gate device.

3. The method of claim 1, wherein:

said input comprises a clock input;

said first-type of signal and said second-type of signal comprise clock trailing edge signals;

said first-type of signal prevents a transition at said output of said gate device due to a transition on a gate inpit of said gate device; and

said second-type of signal causes a transition at said output of said gate device.

4. The method of claim 2, wherein said first-type of signal prevents said clock pulses from being propagated on said output of said gating device and said second-type of signal allows said clock pulses to be propagated on said output of said gating device.

5. The method of claim 2, wherein said sensing time is used in computing a setup test.

6. The method of claim 3, wherein said sensing time is used in computing a hold test.

7. The method in claim 2, wherein said modifying prevents a delay in propagation of said gate signal across said gating device from inappropriately reporting the outputting a portion of a clock pulse.

8. The method of claim 1, wherein said modifying includes assuming there is no load on said output.

9. The method in claim 1, wherein said modifying includes identifying a beginning point of a transition of said first-type of signal as said sensing time.

10. The method of claim 4, wherein the computing of said setup test comprises:

computing a conventional propagated mode test value,

computing an input-to-input test value of zero, and

using the less pessimistic of said computed test values.

11. A method for evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal inhibits a clock pulse from being output from said gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal allows said clock pulse to be output from said gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

12. The method of claim 11, wherein:

said input comprises a gate input;

said first-type of signal and said second-type of signal comprise gating signals.

13. The method of claim 11, further comprising performing a hold test between said input and a clock input of said gating device.

14. The method in claim 11, wherein said modifying prevents a delay in propagation of said gate signal across said gating device from inappropriately reporting the outputting a portion of said clock pulse.

15. The method of claim 11, wherein said modifying includes assuming there is no load on said output.

16. The method in claim 11, wherein said modifying includes identifying a beginning point of a transition of said input toward said first-type of signal as said sensing time of said first-type of signal.

17. A program storage device readable by machine, tangibly embodying a program of instructions executable by said machine for performing a method of evaluating gate timing in an integrated circuit (IC) design, said method comprising:

determining when a first-type of signal is present on an input to a logical gating device, wherein said first-type of input signal inhibits transitions on an output of said gating device;

determining when a second-type of signal is present on said input, wherein said second-type of input signal allows transitions on said output of said gating device; and

modifying a timing of a sensing of said first-type of signal to sense said first-type of signal at an earlier point in time than said second-type of signal is sensed.

18. The program storage device of claim 17, wherein:

said input comprises a gate input;

said first-type of signal and said second-type of signal comprise gating signals; and

said first-type of signal and said second-type of signal control whether pulses on a clock input of said logical gating device are propagated to said output of said gate device.

19. The program storage device of claim 18, wherein said first-type of signal prevents said clock pulses from being propagated on said output of said gating device and said second-type of signal allows said clock pulses to be propagated on said output of said gating device.

20. The program storage device of claim 18, further comprising performing a hold test between said input and said clock input of said gating device.

21. The program storage device in claim 18, wherein said modifying prevents a delay in propagation of said gate signal across said gating device from inappropriately reporting the outputting a portion of a clock pulse.

22. The program storage device of claim 17, wherein said modifying includes assuming there is no load on said output.

23. The program storage device in claim 17, wherein said modifying includes identifying a beginning point of a transition of said input toward said first-type of signal as said sensing time of said first-type of signal.